REMARKS

Claims 1-7, 9-27, and 29-32, and 40-43 were pending. Claims 41 and 43 have been amended. Accordingly, claims 1-7, 9-27, 29-32, and 40-43 remain pending subsequent entry of the present amendment.

Claims 41 and 43 have been amended to generally eliminate redundant language and properly align the recited interrupts and priorities.

Previous Rejections

Applicant notes and appreciates the withdrawal of the previous rejections.

35 U.S.C. § 103 Rejections

In the present Office Action, claims 1-2, 4-7, 9-14, 16-17, 20-24, and 40-43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Motorola MCF5206 Integrated Microprocessor, as described in Freescale Semiconductor, Inc. Product Brief "MCF5206 Integrated Microprocessor" (hereinafter "MCF5206") and Freescale Semiconductor, Inc. "Addendum to MCF5206 User Manual" (hereinafter "MCF5206 Addendum"), in view of US Patent No. 5,025,368 (hereinafter "Watanabe") and newly cited US Patent No. 6,499,078 (hereinafter "Beckert"). Applicant has carefully reviewed the references, including newly cited Beckert, and submits each of the pending claims recite features that are neither disclosed nor suggested in the combination of cited art. Accordingly, Applicant traverses the above rejections and requests reconsideration.

Applicant submits the combination of prior art does not teach or suggest all of the limitations of the claims. For example, claim 1 recites a processing system comprising:

"a plurality of first interrupts generated by a core, said plurality of first interrupts having programmable priorities;

a plurality of second interrupts that are generated external to said core, said second interrupts having architecturally fixed interrupt priorities." (emphasis added).

In the present Office Action, the Examiner states that the above features are taught by the cited art. However, Applicant disagrees and submits none of the cited references alone or in combination disclose "a plurality of second interrupts that are generated external to said core, said second interrupts having architecturally fixed interrupt priorities".

In the Office Action, the examiner suggests the above highlighted features are disclosed in MCF5206. In particular, the examiner cites the following disclosure:

> "Interrupt Controller. The interrupt controller provides user-programmable control of 3 or 7 external interrupt and 5 internal peripheral interrupts. Users can program each internal interrupt to any one of 7 interrupt levels and 4 priority levels within each of these levels. The 3 external interrupt signals can be configured as either fixed interrupt levels 1, 4, and 7, or as a 7-level encoded interrupt. Users can program the external interrupts to any one of the 4 priority levels within the respective interrupt levels." (MCF5206, page 5). (emphasis added).

However, this disclosure of MCF5206 does not teach externally generated interrupts having architecturally fixed interrupt priorities. Rather, the reference clearly teaches the external interrupt signals may be programmed to any of 4 priority levels. Accordingly, the external interrupts of MCF5206 are user-programmable and do not have architecturally fixed interrupt priorities.

Likewise, Beckert discloses only user-programmable priorities of external interrupts, for example Beckert discloses:

> "A hardware-implemented interrupt handler external to a processor handles interrupts destined for the processor. The interrupt handler has a programmable prioritized interrupt array with programmable registers that identify priority levels and handling processes for handling one or more interrupts." (Beckert, Abstract).

> "The interrupt handler 32 implements a prioritized interrupt vector generator that enables the user to program the interrupt priorities and servicing information as desired." (Beckert, col. 3, lines 6-9).

> "The array 40 receives N interrupts 42, as represented by interrupts Int0-Int31, from various sources that provide interrupts to the microprocessor 30." (Beckert, col. 3, line 66 to col. 4 line 2).

In addition, Watanabe merely discloses in its background section that microprocessors have an interrupt controller:

> "Known microprocessors generally comprise a central processing unit (CPU), a random-access memory (RAM), a read-only memory (ROM), an input/output (I/0) unit, an interrupt control register, a timer and so forth." (Watanabe, col. 1 lines 16-20).

Accordingly, none of the cited references disclose architecturally fixed interrupt priorities of the second interrupts as recited, and the combination of cited art does not disclose all the features of claim 1. For at least these reasons, claim 1 is patentably distinguishable from the combination of cited art. As claims 10 and 27 include similar features to those discussed above, each of these claims are patentably distinguishable for similar reasons.

In view of the above discussion, the combination of cited art also does not disclose "a priority encoder, coupled to both said first interrupts and to said second interrupts, and to said status register, said priority encoder prioritizing said first and second pluralities of interrupts utilizing said programmable priorities for said first interrupts and said architecturally fixed interrupt priorities for said second interrupts." As

the combination of art does not disclose these features, each of independent claims 1, 10 and 27 are patentably distinguishable for at least these additional reasons.

As each of the dependent claims include the features of the independent claims on which they depend, each of the dependent claims are patentably distinct from the cited art, taken either singly or in combination, for at least the above reasons.

Finally, as noted in Applicant's previous reply, Applicant does not agree with the examiner's proposed motivation for combining the cited references. As the combination does not disclose all the features of the claims as discussed above, Applicant does not believe it necessary to revisit the motivation argument at this time. For purposes of economy, Applicant's previous comments are incorporated herein by reference.

In view of the above, Applicant submits the claims are patentably distinct from the combination of cited art. Accordingly, Applicant respectfully requests withdrawal of the rejections.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

Respectfully submitted,

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Date: 4/25/2007